ABSTRACT OF THE DISCLOSURE

A method of mapping logic failures in an integrated circuit die includes steps of: (a) generating a navigation map of test paths for an integrated circuit die; (b) selecting a grid spacing to define a grid map of cell locations from the navigation map for each of the test paths; and (c) calculating a value for each of the cell locations wherein the value is representative of the difference between a total number of the test paths intersecting each of the cell locations and a failed number of the test paths intersecting each of the cell locations.